WHAT IS CLAIMED IS:

1. A method for detecting quiescent current in an integrated circuit, comprising:

detecting a magnetic field generated by the quiescent current and in response generating a magnetic field signal that is indicative of the detected magnetic field;

amplifying the magnetic field signal;

converting the magnetic field signal into a differential voltage signal; and

converting the differential voltage signal into a digital format.

2. The method of Claim 1, wherein converting the differential voltage signal to a digital format comprises converting the differential voltage signal into a digital bit stream that is communicated to a counter such that an accumulated result is generated in the counter, the accumulated result representing the approximate Gaussian distribution of the magnetic field signal.

3. The method of Claim 2, wherein conversion of the differential voltage signal into the digital bit stream is performed using a stochastic process that repeatedly compares the differential voltage signal and background noise and that amplifies the difference between the differential voltage signal and the background noise.

4. The method of Claim 1, further comprising scanning out the converted differential voltage in its digital format to a processing element.

5. The method of Claim 1, further comprising receiving the differential voltage signal at one or more flip flops, each of the flip flops operable to compare the differential voltage signal and background noise and in response to the comparison flip in order to produce a selected binary digit.

6. The method of Claim 5, further comprising receiving and reading the selected binary digit with a data detector operable to provide a signal to a counter based on the operation of the flip flop, the counter operable to store a digital bit stream that reflects a series of comparisons between the differential voltage signal and the background noise.

7. The method of Claim 1, further comprising executing a calibration cycle before initiating detection of the magnetic field generated by the quiescent current, the calibration cycle comprising a plurality of clock cycles that generate a zero magnetic field signal that produces a magnetic field sensing equilibrium before detection of the magnetic field commences.

8. An apparatus for detecting quiescent current in an integrated circuit, comprising:

a magnetic field sensing element operable to detect a magnetic field generated by the quiescent current and to generate a magnetic field signal indicative of the magnetic field, the magnetic field sensing element being further operable to amplify the magnetic field signal and convert the magnetic field signal into a differential voltage signal; and

a stochastic sensor operable to convert the differential voltage signal into a digital format.

9. The apparatus of Claim 8, wherein the magnetic field sensing element is a magnetic field effect transistor (MAGFET) sensor.

10. The apparatus of Claim 9, wherein the MAGFET sensor comprises two P-type and two N-type MAGFETs.

11. The apparatus of Claim 10, wherein the P-type and N-type MAGFETs are arranged in a cross-coupled configuration and oriented such that in the presence of the magnetic field a drain associated with a selected one of the P-type MAGFETs having an increased current as a result of the magnetic field is coupled to a drain associated with a selected one of the N-type MAGFETs having a decreased current as a result of the magnetic field.

12. The apparatus of Claim 9, further comprising a low-pass filter coupled to a selected one or more of a plurality of MAGFET sensor outputs, the low-pass filter operable to reduce noise.

13. The apparatus of Claim 8, further comprising a counter operable to receive a digital bit stream that reflects a comparison between the differential voltage signal and background noise.

14. The apparatus of Claim 13, further comprising a processing element operable to scan out the digital bit stream that reflects a comparison between the differential voltage signal and background noise.

15. The apparatus of Claim 8, wherein the stochastic sensor executes a stochastic process that repeatedly compares the differential voltage signal and background noise and that amplifies the difference between the signal and the background noise for further processing.

16. The apparatus of Claim 15, wherein the stochastic sensor comprises one or more flip flops operable to receive the differential voltage signal, each of the flip flops operable to compare the differential voltage signal and background noise and in response to the comparison flip in order to produce a selected binary digit.

17. The apparatus of Claim 16, wherein the stochastic sensor further comprises a data detector operable to receive and to read the selected binary digit, the data detector being further operable to provide a signal to a counter based on the operation of the flip flop, the counter storing a digital bit stream that reflects a series of comparisons between the differential voltage signal and the background noise.

18. The apparatus of Claim 15, further comprising a counter operable to receive a digital bit stream that reflects a comparison between the differential voltage signal and background noise.

19. The apparatus of Claim 18, further comprising a processing element operable to scan out the digital bit stream that reflects a comparison between the differential voltage signal and background noise.

20. The apparatus of Claim 15, wherein the stochastic sensor further comprises a calibration tool operable to execute a calibration cycle before initiating detection of the magnetic field generated by the quiescent current, the calibration cycle comprising a plurality of clock cycles that generate a zero magnetic field signal that is fed to internal components of the stochastic sensor such that a magnetic field sensing equilibrium is reached.

21. A method for detecting quiescent current in an integrated circuit, comprising:

detecting a magnetic field generated by the quiescent current and in response generating a magnetic field signal that is indicative of the detected magnetic field;

amplifying the magnetic field signal;

converting the magnetic field signal into a differential voltage signal;

converting the differential voltage signal into a digital bit stream using a stochastic process that repeatedly compares the differential voltage signal and background noise and that amplifies the difference between the differential voltage signal and the background noise, the digital bit stream being communicated to a counter such that an accumulated result is generated in the counter, the accumulated result representing the approximate Gaussian distribution of the magnetic field signal; and scanning out the digital bit stream to a processing element.

22. An apparatus for detecting quiescent current in an integrated circuit, comprising:

a magnetic field effect transistor (MAGFET) sensor that comprises two P-type and two N-type MAGFETs and that is operable to detect a magnetic field generated by the quiescent current and to generate a magnetic field signal indicative of the magnetic field, the MAGFET sensor being further operable to amplify the magnetic field signal and convert the magnetic field signal into a differential voltage signal, wherein the MAGFETs are arranged in a cross-coupled configuration and oriented such that in the presence of the magnetic field a drain associated with a selected one of the P-type MAGFETs having an increased current as a result of the magnetic field is coupled to a drain associated with a selected one of the N-type MAGFETs having a decreased current as a result of the magnetic field;

a stochastic sensor operable to convert the differential voltage signal into a digital format;

a counter operable to receive a digital bit stream that reflects a comparison between the differential voltage signal and background noise; and

a processing element operable to scan out the digital bit stream that reflects a comparison between the differential voltage signal and background noise.

23. An apparatus for detecting quiescent current in an integrated circuit, comprising:

a magnetic field sensing element operable to detect a magnetic field generated by the quiescent current and to generate a magnetic field signal indicative of the magnetic field, the magnetic field sensing element being further operable to amplify the magnetic field signal and convert the magnetic field signal into a differential voltage signal; and

a stochastic sensor operable to convert the differential voltage signal into a digital format, wherein the stochastic sensor executes a stochastic process that repeatedly compares the differential voltage signal and background noise and that amplifies the difference between the signal and the background noise for further processing, and wherein the stochastic sensor comprises one or more flip flops operable to receive the differential voltage signal, each of the flip flops operable to compare the differential voltage signal and background noise and in response to the comparison flip in order to produce a selected binary digit.

24. An integrated circuit, comprising:

a quiescent current detection system, the system comprising:

a magnetic field effect transistor (MAGFET) sensor that comprises two P-type and two N-type MAGFETs and that is operable to detect a magnetic field generated by the quiescent current and to generate a magnetic field signal indicative of the magnetic field, the MAGFET sensor being further operable to amplify the magnetic field signal and convert the magnetic field signal into a differential voltage signal, wherein the MAGFETs are arranged in a cross-coupled configuration and oriented such that in the presence of the magnetic field a drain associated with a selected one of the P-type MAGFETs having an increased current as a result of the magnetic field is coupled to a drain associated with a selected one of the N-type MAGFETs having a decreased current as a result of the magnetic field,

a stochastic sensor operable to convert the differential voltage signal into a digital format,

a counter operable to receive a digital bit stream that reflects a comparison between the differential voltage signal and background noise, and

a processing element operable to scan out the digital bit stream that reflects a comparison between the differential voltage signal and background noise.

25. An integrated circuit, comprising:

a quiescent current detection system, the system comprising:

a magnetic field sensing element operable to detect a magnetic field generated by the quiescent current and to generate a magnetic field signal indicative of the magnetic field, the magnetic field sensing element being further operable to amplify the magnetic field signal and convert the magnetic field signal into a differential voltage signal, and

a stochastic sensor operable to convert the differential voltage signal into a digital format, wherein the stochastic sensor executes a stochastic process that repeatedly compares the differential voltage signal and background noise and that amplifies the difference between the signal and the background noise for further processing, and wherein the stochastic sensor comprises one or more flip flops operable to receive the differential voltage signal, each of the flip flops operable to compare the differential voltage signal and background noise and in response to the comparison flip in order to produce a selected binary digit.

26. An apparatus for detecting quiescent current in an integrated circuit, comprising a stochastic sensor operable to receive a differential voltage signal indicative of a quiescent current generated by the integrated circuit, wherein the stochastic sensor converts the differential voltage signal into a digital format that represents a digital value associated with the quiescent current.

27. The apparatus of Claim 26, wherein the stochastic sensor executes a stochastic process that repeatedly compares the differential voltage signal and background noise and that amplifies the difference between the signal and the background noise for further processing.

28. The apparatus of Claim 26, wherein the stochastic sensor comprises one or more flip flops operable to receive the differential voltage signal, each of the flip flops operable to compare the differential voltage signal and background noise and in response to the comparison flip in order to produce a selected binary digit.

29. The apparatus of Claim 28, wherein the stochastic sensor further comprises a data detector operable to receive and to read the selected binary digit, the data detector being further operable to provide a signal to a counter based on the operation of the flip flop, the counter storing a digital bit stream that reflects a series of comparisons between the differential voltage signal and the background noise.

30. The apparatus of Claim 26, further comprising a counter operable to receive a digital bit stream that reflects a comparison between the differential voltage signal and background noise.

31. The apparatus of Claim 30, further comprising a processing element operable to scan out the digital bit stream that reflects a comparison between the differential voltage signal and background noise.

32. The apparatus of Claim 26, wherein the stochastic sensor further comprises a calibration tool operable to execute a calibration cycle, the calibration cycle comprising a plurality of clock cycles that generate a zero magnetic field signal that is fed to internal components of the stochastic sensor such that a magnetic field sensing equilibrium is reached.